Associative Memory via Memristive Neural Networks

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Abstract: This paper investigates associative memory based on memristive neural networks. Based on the reproducible gradual resistance tuning in bipolar mode, a first-order voltage-controlled memristive model is employed with asymmetric voltage thresholds. Since memrisive devices are especially tiny to be densely packed in crossbar-like structures and possess long time memory needed by neuromorphic synapses, this paper shows how to approximate the behavior of synapses in neural networks using this memristive device. Certain neural networks are established and applied in associative memory.

Key words: Memristor; associative memory; neural networks

0 Introduction

The sequential processing of fetch, decode, and execution of instructions through the classical von Neumann bottleneck of conventional digital computers has resulted in less efficient machines as their eco-systems have grown to be increasingly complex [1]. Though the current digital computers can now possess the computing speed and complexity to emulate the brain functionality of animals like a spider, mouse, and cat [2,3], the associated energy dissipation in the system grows exponentially along the hierarchy of animal intelligence. Therefore, it is very critical to build a brain-like machine.

On the other hand, it has long been hindered by challenges related to area and power consumption restrictions to implement neuromorphic circuits and chips. More than tens of transistors and capacitors are needed to estimate a synapse [4]. In particular, when neural connections becomes high level, a large part of neuromorphic chips is utilized for synapses, whereas neurons take only a small portion compared to that of synapses. However, shrinking the current transistor size is very difficult. Therefore, it is essential to introduce a more efficient approach to implement neuromorphic circuits and chips.

Memristors, as the fourth electrical elements theoretically proposed by Leon Chua in 1971 [5], are two-terminal electronic devices that memorize the flowing charge. In fact, they are resistive in essence, but their resistance can be altered electrically with nonlinear properties. Since the first realization of a working memristor was announced in a Pt/TiO2/Pt by Hewlett-Pakard Laboratories [6], memristors and memristive devices have been widely investigated and discussed for their prospective applications in nonvolatile memories [7,8], logic devices [9,10], neuromorphic devices [1, 11, 12], and neuromorphic self-organized computation and learning [13,14]. Furthermore, researchers have packed memristors into crossbars to form dense memories [15], and designed integrated circuitry compatible with CMOS processes [16]. All these will make memristors potential to be integrated with conventional integrated circuitry. Although the state of memristor will decay over time, the time constant can be as long as weeks to decades. All these make the

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memristors candidates to be used as synaptic circuits.

1 Neuromorphic Learning and Circuit Implementation

A typical crossbar-structure A-GST based memristor is fabricated by micro/nano processes as shown in Fig. 1. A-GST is sandwiched between Cu and Cu/Ag, where Ag layer serves as the cation source. This two terminal device can be used as a neuromorphic synapse. And an electrical system is built up to perform electrical measurements. The states of this device can be switched to amorphous or crystalline ones. To investigate the memristance of A-GST, this memristive device is first set to behavior in crystalline state. Then, the memristive behavior can be observed in crystalline-GST under clockwise voltage sweep 0.6 V →-1.5 V→ 0.6 V$, as demonstrated in Fig 1.

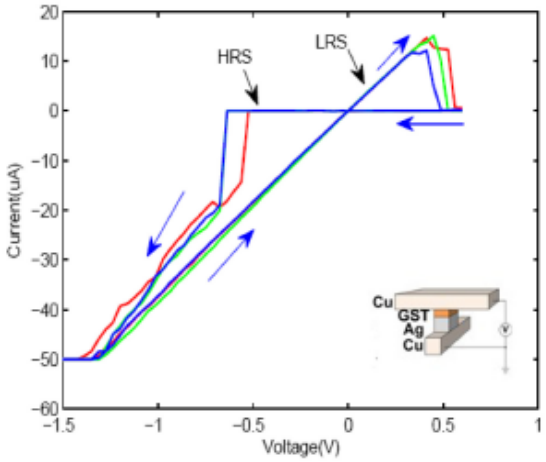

Fig. 1 CI-V characteristics of the device, exhibiting a memristive hysteresis loop. The blue arrows show the directions of sweeping voltage, and HRS and LRS represent high and low resistance states respectively.

It is obvious that the resistance can be modulated with a certain range via switching the voltage polarity. The lowest resistance state (LRS) is below 3KΩ, while the highest resistance state (HRS) is over 18KΩ. And the switching voltage is 0.35V. To simplify the model of the A-GST memristive device, a threshold memristive model is considered as follows:

$$\begin{aligned} &I = M^{-1}V_M, \\ &\dot{M} = f(V_M)[\theta(\frac{M}{R_1}-1)+\theta(-V_M)\theta(1-\frac{M}{R_2})], \\ &f(V) = -\beta V + \frac{\beta-\alpha}{2}(|V+V_L|-|V-V_R|+V_R-V_L), \end{aligned} \tag{1}$$

where I and V_M represent the current through and voltage drop on the device, respectively, M is the internal state variable as the memistance R, α and β characterize the rate of memristance change when $|V_M|$ is less or greater than threshold voltage, respectively, there V_L and V_R are threshold voltages, and the unit step functions $\theta(.)$ guarantee the memristance can change only between R_1 and R_2.

Based on the threshold feature, Querlioz et al investigated immunity to device variations in a spiking neural network with memristive nanodevices, Gao et al proposed a hybrid

CMOS/memristor implementation of a programmable threshold logic gate. These mentioned works develop a new way to investigate in the application field of memristive devices. Based on these excellent works, this paper proposes a scheme to realize real-time monitor of the memristor state and off-line training in the case that directly programming the resistance of a single memristor to the target value is likely impossible.

As memristor can record the electrical excitations on itself and occur corresponding resistance change like the biologic synapses with very little decay for long periods of time. Several breakthroughs have been motivated in the design of memristive neuromophic systems and neural networks [1]. However, it is difficult to realize real-time monitoring the memristor state and off-line training, as directly programming the resistance of a single memristor to the target value is likely impossible. Then it is necessary to discretely implement the memristive synapses in order to maximize noise immunity, minimize power dissipation and so on. Therefore, it is particularly desirable to implement the weights by with binary memristive devices that communicate via spikes rather than analog voltages, as biology itself takes discrete spikes to communicate. Hence, a scheme is needed to approximate continuous signals and models with discrete ones.

Based on the threshold A-GST memristive device, each A-GST memristive device is used to store a single bit, such as using HRS to present a logic 0 bit value, and the LRS to present a logic 1 bit value. As the existence of threshold voltages, these devices can be rapidly altered their resistance, and low voltages have negligible effect on this kind of memristive devices, while larger voltages can make them rapidly change their resistance. Therefore, a positive voltage more than the positive On threshold will make A-GST memristive devices switch into the LRS, meanwhile, a negative voltage below the negative Off threshold will make A-GST switch into HRS. When an analog voltage input x drops through an A-GST memristive synapse which memconductive is ω, we can get the output

$$y = \omega x \tag{2}$$

And an abstract circuit is given to implement memristive synapses in Fig. 2. This schematic is a clocked or synchronous circuit that is evaluated at discrete-time steps. First, the continuous analog input signal x is transformed to a discrete digital approximation by a Thermometer code. This coding method can convert the analog signals within the range [0,1] into a discrete version. Although this encoding is less efficient than a binary numerical one, it is much simpler to be implemented.

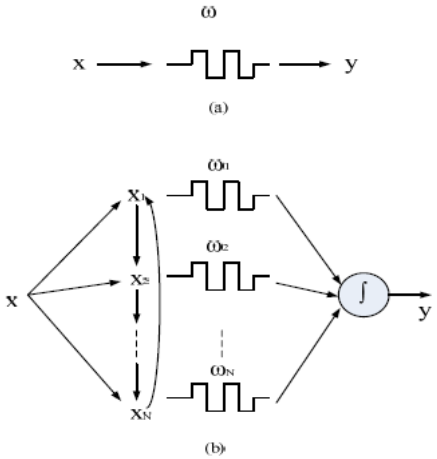

Fig 2 (a) memristive synapse, (b) discrete approximation implementation of this synapse, much of this circuitry can be shared by multiple synapses.

To implement the circuit in Fig. 2, an analog input x is encoded by thermometer code to produce the code vector $(x_1,\cdots,x_N)$, which is parallel sent to a circular shift register. Then, this shift register is clocked N times to send $spikes$ through the binary switches ω_i to an integrator which accumulates the spikes weighted in variable y.

For a single memristive switch as show in Fig. 3, during the evaluation of the transfer function, S_1 is switched to state position and S_2 is closed. A narrow spike is sent in each step when $x_i=1$, otherwise, no spike is sent when $x_i=0$, and these spikes are below the threshold voltages that can not alter the value of the A-GST memristive device. And during the learning stage, which occurs at last in a major cycle, S_1 is switched to learn position, $f(x_i)$ and $g(x_i)$ cooperate to refresh the state of ω_i. S_2 keeps closed in order to discharge the integrator and reset variable y to 0.

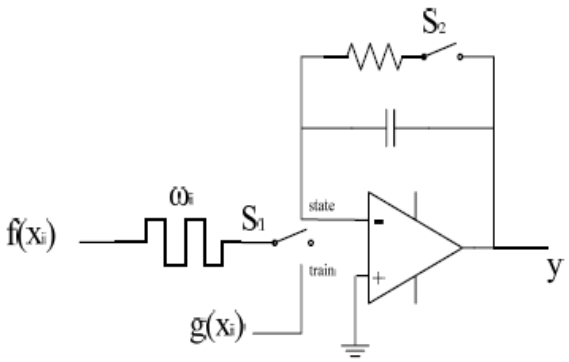

Fig 3 Circuit implementation of a single memristive switch.

To implement Fig. 2, each major cycle is divided into $N+1$ steps as shown in Fig. 4. The first N steps are used to implement the evaluation of the transfer function an approximation of the desired output signal $x\omega$ can be computed, and the final step is used to implement the synaptic weight update.

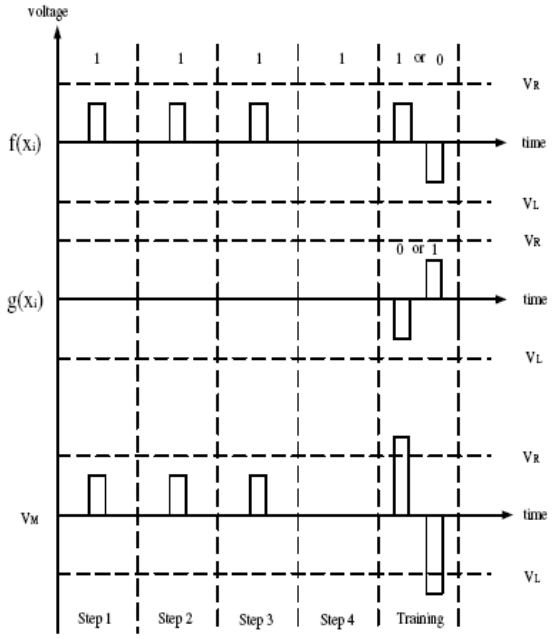

Fig 4 Circuitry input signals $f(x_i)$ and $g(x_i)$ ($N=4$).

2 Memristive Neural networks and Applications

Based on A-GST memristive devices, an artificial neural network is designed to learn and recognize standard patterns as in Fig. 5, where input and output layer neurons are connected by the A-GST memristive devices as neuromorphic synapses. Via these synapses, the output layer neurons collect the information from the input layer neurons with certain activation functions.

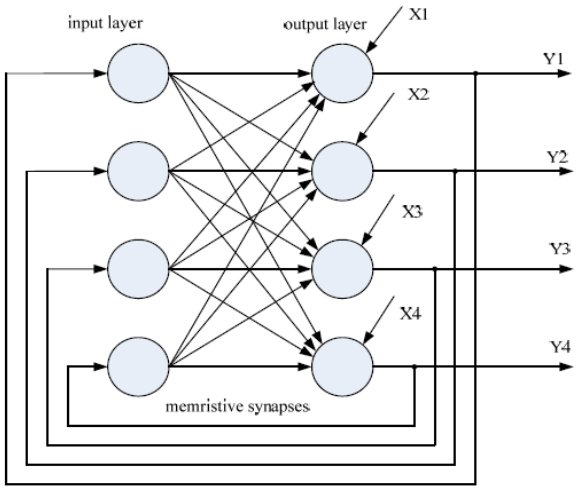

Fig 5 Schematic of artificial neural networks with memristive synapses. All circuitry for an input/output neuron can be shared by all memristive synapses connecting to it, so it is obvious to obtain a high-density circuit of neural networks.

And the process to train the memristive neural networks is defined as the programming the memristance which represents the connection weights. In general, there are two ways to train these networks such as direct open loop training method and close loop training method. During the training process, the connection weights are updated iteratively until the difference between the output and the target output reaches the minimum.

After being trained to memorize standard numbers 1, 2 and 3, the A-GST memristive neural

networks can recognize certain input noisy samples through associative memory as shown in Fig. 6.

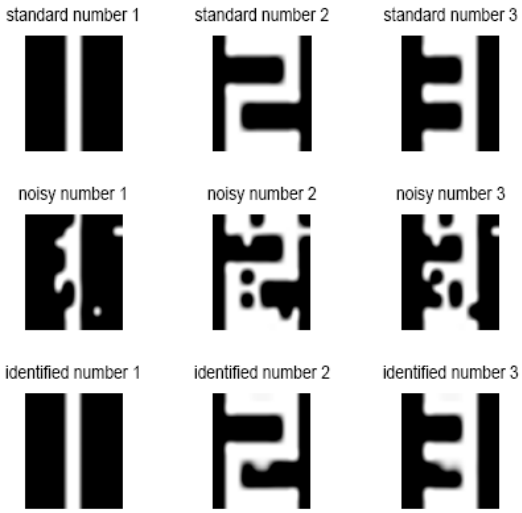

Fig 6 Simulation results of memristive neural networks for recognition of digital numbers.

3 Discussion and Summary

Neural networks are used widely in different areas such as combinatorial optimization, knowledge acquisition and pattern recognition. Training such systems involves adjusting the weight between the two neurons it connects. And memory is needed to hold the synaptic weights; and if the memory were volatile, then in the case of power loss, what have been learned will be lost. Storing synaptic weights in external, nonvolatile memory, such as flash, would involve both of those problems, and need high bandwidth as each weight has to be read on each cycle to implement the calculation with power loss to transmit the weight information across chip boundaries. Then it deserves to investigate how synapses can be trained and stored learning information without external memory.

A-GST memristive devices provide a preferable choice as they are non-volatile, nanoscale, can be fabricated with CMOS circuitry and to form dense memories in crossbars. A scheme is given in this paper to exploit the features to build such neuromorphic synapses, and this will promote the development of neuromorphic integrated circuitry which are close to the level of biological density and power.

In summary, this paper concerns several problems in the design of memristive neural networks to take A-GST memristive devices to immunity the variation and perturbation problems and realize real-time monitor of the memristor state and off-line training. And this will promote the development of neuromorphic integrated circuits to imitate biological-scale brains.

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基于忆阻神经网络的联想记忆

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摘要：本文研究了基于忆阻神经网络的联想记忆。根据忆阻器二极模型的阻值的可变性，提出一种带有非对称电压阈值一维电压控制模型。由于忆阻设备尺寸非常的小可以集成到阵列结构中去，且具有神经突触所需的长时存储功能，本文研究如何利用忆阻设备来模拟神经网络突触的行为特性，建立相应的忆阻神经网络，并用于实现联想记忆。

关键词：忆阻器；联想记忆；神经网络
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